REMARKS

Claims 1 through 8 are currently pending in the application.

This amendment is in response to the Office Action of June 19, 2002.

Claims 1 through 8 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1 and 2 of United States Patent 5,539,324. In order to avoid further expenses and time delay, Applicants elect to expedite the prosecution of the present application by filing a terminal disclaimer to obviate the double patenting rejection in compliance with 37 C.F.R. §1.321 (b) and (c). Applicants' filing of the terminal disclaimer should not be construed as acquiescence of the Examiner's double patenting or obviousness-type double patenting rejection. Attached is the terminal disclaimer and accompanying fee.

Claims 1 through 8 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Madden, Enochs, Corbett et al. or Lee et al. in a first set in view of Elder et al. in a second set.

After carefully considering the cited prior art, the rejections, and the Examiner's comments, Applicants have amended the claimed invention to clearly distinguish over the cited prior art.

Applicants further submit that to establish a *prima facie* case of obviousness under 35 U.S.C. § 103 three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Third, the cited prior art reference must teach or suggest all of the claim limitations. Furthermore, the suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on Applicants' disclosure.

Madden describes an arrangement for solderless mounting of an integrated circuit chip carrier on a printed wiring board. A leadless chip carrier is fitted within a socket cemented to the board. A contact interface element with an array of electrically conductive annular springs electrically connect the contact pads of the chip carrier and the contact pads of the printed wiring

board. The interface element is clamped between the chip carrier and the board by a compression spring on the upper surface of the chip carrier.

Enochs describes a pressure interconnect package for connecting an integrated circuit chip to an etched circuit board by applying a certain amount of compression to a top plate in order that it may be twist locked onto a base such that certain conductive portions in a stack of relatively flat elements are aligned on the base to make electrical contact. The package comprises a stack of circuit elements, retainer members, and pressure pads. The stack is then threaded onto alignment members and a top plate. Top plate is threaded over the members on top of the stack and twist locked into place (Col. 1, lines 39-54).

Corbett et al describes a reusable burn-in/test fixture for discrete TAB die. The fixture consists of two halves, one is *a die* cavity plate for receiving semiconductor dice as the units under test (UUT) and the other half is a probe plate which establishes electrical contact with the dice and with a burn-in oven. The die cavity plate includes a plurality of die receiving cavities, each of which is in dimension to receive *a semiconductor die.* Each die receiving cavity includes a floating platform which is supported by a spring mechanism. In contrast to the present invention, Corbett et al. relates to a technique for *testing individual die.*

In contrast to Corbett et al., the present invention teaches a technique using a burn-in/test fixture for testing *a plurality of semiconductor dice in an uncut wafer form.*

Lee describes a semiconductor mounting system provided for detachable surface mounting of one or more semiconductor dies on a conductor substrate such as a printed circuit board. The system uses a conductor pad that is interposed between the semiconductor die and the conductor substrate. Electrical contact is established between contacts on the semiconductor die and corresponding contacts on the conductor substrate by pressing the semiconductor die and conductor pad against the conductor substrate.

Elder describes a burn-in test socket for integrated circuit die during testing. The test fixture has three components. The first is a flexible probe head which provides the electrical contact between the bond pads on the semiconductor die and the rest of the test socket. The

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second part is a Pin Grid Array package to which probe head is attached. The third part of the test fixture is a heat sink and clamp mechanism which holds the device under test in place and cools the die while holding the test socket together. Although the test socket can be used for testing complete wafers, the test fixture is comprised of components that are very different from the components comprising a wafer testing apparatus described and claimed in the present invention. Therefore, it would be inappropriate to use such a reference in combination with other cited references to render the present invention obvious.

Independent claim 1, as amended herein, recites a testing apparatus for a *wafer* of semiconductor dice which includes, among other things, "a first rigid support member for receiving a plurality of semiconductor dice in wafer form having a predetermined orientation", "a second rigid support member for selectively engaging the first rigid support member to retain the plurality of semiconductor dice in wafer form therebetween", "one of the first rigid support member and the second rigid support member including *a single cavity for retaining said plurality of semiconductor dice in wafer form therein during testing*" as well as "a single biasing assembly including a *single floating platform* of a preselected area substantially sized for the single cavity...the single biasing assembly sized for *uniformly biasing the plurality of semiconductor dice in wafer form*." Applicant submits that any combination of the cited prior art under the provisions of 35 U.S.C. § 103 does not include such claim limitations. Therefore, since any combination of the cited prior art does not teach or suggest each and every claim limitation of independent claim 1, it is respectfully submitted that claim 1, as proposed to be amended, is not rendered obvious by the cited prior art to establish a *prima facie* case of obviousness under 35 U.S.C. § 103.

Independent claim 6, as amended herein, recites a wafer testing apparatus which includes among other things "a first rigid support member and a second rigid support member for receiving *a plurality of semiconductor dice on a wafer therebetween*, one of the first rigid support member and second rigid support member including *a single cavity for retaining said plurality of semiconductor dice on a wafer therein during testing*", "a single biasing assembly

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including *a single floating platform* having a preselected area substantially sized to correspond with the single cavity *and an elastomeric member* disposed on the second rigid support member" as well as "the single biasing assembly sized for uniformly biasing said plurality of semiconductor dice on a wafer."

Applicant submits that none of the cited prior art, taken alone or in any combination, teaches or suggests the claim limitations as specifically claimed in presently amended independent claim 6 to establish a *prima facie* case of obviousness under 35 U.S.C. § 103. Therefore, it is respectfully submitted that independent claim 6, as proposed to be amended, is allowable over the cited prior art, taken alone or in combination under 35 U.S.C. § 103.

While Patent Office classification of references may be some evidence of analogy, Applicant submits that "the similarities and *differences in structure* and function of the inventions [should] carry far greater weight [in combining references for an obvious rejection]," *In re Ellis,* 476 F.2d 1370, 1372, 177 USPQ 526, 527 (CCPA 1973).

Applicant submits that it is clear that the structural differences between the cited references Madden, Lee, Corbett, Enochs and Elder and the presently claimed invention are very significant. Therefore, it would be inappropriate to combine such references in order to attempt to establish a *prima facie* case of obviousness under 35 U.S.C. § 103 regarding the presently claimed invention.

Claims 2 through 5, 6 and 7 are each allowable as depending from presently amended independent claims 1 and 6, which are allowable.

Moreover, Applicant respectfully submits that one of ordinary skill in the art, at the time the referenced application was filed, would not have been motivated to modify or combine the teachings of the cited prior art in the manner that has been set forth in the outstanding Office Action to establish a *prima facie* case of obviousness under 35 U.S.C. § 103 regarding subject matter of the presently claimed invention of claims 1 through 8.

Applicant further submits that the knowledge generally available in the art at the time the present application was filed would also have failed to provide one of ordinary skill in the art

with any suggestion or motivation to modify or combine the teachings in the cited prior art to establish a *prima facie* case of obviousness under 35 U.S.C. § 103 regarding the presently claimed invention.

For each of the foregoing reasons, Applicants respectfully submit that, under 35 U.S.C. § 103(a), claims 1 through 8 are clearly allowable over the cited prior art.

Applicants respectfully request the allowance of claims 1 through 8 and the case passed for issue.

Respectfully submitted,

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Date: September 19, 2002

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Enclosure: Version with Markings to Show Changes Made

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APPENDIX A

VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE CLAIMS:

A marked-up version of each of the presently amended claims, highlighting the changes thereto, follows:

1. (Twice Amended) A testing apparatus for a wafer of semiconductor dice comprising:

a first rigid support member for receiving a plurality of semiconductor dice in wafer form having a predetermined orientation, the first rigid support member having a plurality of contact members thereon and having a plurality of electrical connectors connected to the contact members for establishing communication with test circuitry;

a second rigid support member for selectively engaging the first rigid support member to retain the plurality of semiconductor dice in wafer form therebetween, one of the first rigid support member and the second rigid support member including a single cavity for retaining [the] said plurality of semiconductor dice in wafer form therein during testing; and

a single biasing assembly including a single floating platform of a preselected area substantially sized for the single cavity, the single biasing assembly mounted to one of the first rigid support member and second rigid support member, the single biasing assembly sized for uniformly biasing the plurality of semiconductor dice in wafer form against the contact members.

6. (Twice Amended) A wafer testing apparatus comprising:

a first rigid support member and a second rigid support member for receiving a plurality of semiconductor dice on a wafer therebetween, one of the first rigid support member and second rigid support member including a single cavity for retaining [the] said plurality of semiconductor dice on a wafer therein during testing;

a plurality of contact members formed on the first rigid support member for communicating with electrical connectors for connecting to external test circuitry;

a single biasing assembly including a single floating platform having a preselected area substantially sized to correspond with the single cavity and an elastomeric member disposed on the second rigid support member, the single biasing assembly sized for uniformly biasing [the] said plurality of semiconductor dice on a wafer towards the contact members, the single floating platform directly supporting the wafer with the elastomeric member sandwiched between the single floating platform and the second rigid support member.

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